











- ☐ Drafts
- ☐ Pending
- ☒ Active
 - ☒ L1: (2) ("20020054309").PN.
 - ☒ L2: (7514) network adj processor
 - ☒ L3: (111700) cache
 - ☒ L4: (743088) cam or (content adj address\$4 adj memory)
 - ☒ L5: (233) 2 and 3 and 4
 - ☒ L6: (22) 2 same 3 same 4
 - ☒ L7: (21980) shared adj memory
 - ☒ L9: (61) 8 not 6
 - ☒ L8: (63) 2 and 3 and 4 and 7
- ☐ Failed
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- ☐ UDC
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	U	1	Document ID	Issue Date	Pages	Inventor	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030009651 A1	20030109	40	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to	712/34	
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030147409 A1	20030807	13	Wolrich, Gilbert et al.	Processing data packets	370/412	
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20050268072 A1	20051201	35	Najam, Zahid et al.	Apparatus and method for interconnecting a processor to	712/34	
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6311212 B1	20011030	10	Chong, Simon et al.	Systems and methods for on-chip storage of virtual connection	709/212	365/49;
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 7082502 B2	20060725	31	Najam, Zahid et al.	Apparatus and method for interfacing with a high speed bi-directional	711/147	370/202; 709/213; 709/253

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-  Saved
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